WE CLAIM:

1. An enhanced T-gate comprising:

a free T-gate, said free T-gate having a neck portion, said neck portion having a height, and a T-bar portion, said T-bar portion having overhangs extending beyond said neck portion by a first width; and

an insulator layer disposed on each side of said neck portion, forming a sandwich structure with said neck portion along a width direction of said free T-gate, and wherein said insulator layer only partially filling up a volume defined therebetween said overhangs and a surface on which said free T-gate is standing.

2. The enhanced T-gate of claim 1, wherein in said sandwich structure said insulator layer creating spacers on each side of said neck portion, wherein said spacers having a second width, said second width being less than said first width of said overhangs, whereby that part of said volume which is further from said neck portion than said second width is not filled with said insulators.

3. The enhanced T-gate of claim 1, wherein in said sandwich structure said insulator layer having approximately a C-shape, conformally adhering to a bottom surface of said overhangs, to said neck portion, and to said surface on which said free T-gate is standing, said insulator layer having a thickness which is less than half of said height of said neck

portion, wherein said insulator layer covering said surface on which said free T-gate is standing and said bottom surface of said overhang to a distance from said neck portion substantially equal to said first width, whereby that part of said volume which is inside said C-shape is not filled by said insulator.

4. The enhanced T-gate of claim 1, wherein said insulator layer is a low-k material.

5. The enhanced T-gate of claim 4, wherein said low-k material is a compound of materials selected from the group consisting of SiCO, SiCOH, SiCH, these silicon containing materials with Si up to 100% replaced by Ge and these silicon containing materials further containing atoms of materials selected from the group consisting of N and F.

6. The enhanced T-gate of claim 4, wherein said low-k material is selected from the group consisting of diamond-like carbon, fluorinated amorphous carbon, insulating inorganic oxides, inorganic polymers, organic polymers, photosensitive organic materials, fluorinated organic materials, other carbon-containing materials, hybrid organo-inorganic materials and silsesquioxane-based materials.

7. A MODFET device comprising an enhanced T-gate, said enchanted T-gate further comprising:

a free T-gate, said free T-gate having a neck portion and a T-bar portion, said T-bar portion having overhangs extending beyond said neck portion; and

an insulator layer disposed on each side of said neck portion, forming a sandwich structure with said neck portion along a width direction of said free T-gate, and wherein said insulator layer only partially filling up a volume defined therebetween said overhangs and a surface on which said free T-gate is standing.

8. The MODFET device of claim 7, further comprising a self-aligned source/drain metallurgy, wherein a borderline of said metallurgy is defined by said insulator layer.

9. An integrated circuit comprising at least one MODFET device, said MODFET device comprising an enhanced T-gate, wherein said enchanted T-gate further comprising:

a free T-gate, said free T-gate having a neck portion and a T-bar portion, said T-bar portion having overhangs extending beyond said neck portion; and

an insulator layer disposed on each side of said neck portion, forming a sandwich structure with said neck portion along a width direction of said free T-gate, and wherein said insulator layer only partially filling up a volume defined therebetween said overhangs and a surface on which said free T-gate is standing.

10. The integrated circuit of claim 9, wherein said at least one MODFET further comprising a self-aligned source/drain metallurgy, wherein a borderline of said

metallurgy is defined by said insulator layer.

11. The integrated circuit of claim 9, further comprising a multilevel interconnect structure of low-k interconnect dielectrics.

12. The integrated circuit of claim 11, wherein said low-k interconnect dielectrics leaving voids in said volume only partially filled up by said insulator layer.

13. The integrated circuit of claim 11, wherein said low-k interconnect dielectrics are materials selected from the group consisting of SiCO, SiCOH, SiCH, these silicon containing materials with Si up to 100% replaced by Ge, diamond-like carbon, fluorinated amorphous carbon, insulating inorganic oxides, inorganic polymers and organic polymers.

14. A method for producing an enhanced T-gate, comprising the steps of:

fabricating a free T-gate, said free T-gate having a neck portion and a T-bar portion;

coating conformally said free T-gate with an insulator; and

removing anisotropically said insulator by using said T-bar portion for masking, wherein leaving said insulator only underneath said T-bar portion, whereby said insulator forming sidewalls around said neck portion.

15. The method of claim 14, wherein the step of conformally coating further comprises the step of adjusting a thickness of said insulator, wherein said thickness controls a width of said sidewalls.

16. The method of claim 14, wherein the step of conformally coating is executed by selecting a technique from the group consisting of: chemical vapor deposition (CVD), plasma-enhanced CVD (PECVD), plasma polymerization, hot-filament-assisted CVD, high-density-plasma PECVD, sputter deposition, reactive sputter deposition, ion beam deposition, spinning from solution, spraying from solution and dipping.

17. The method of claim 14, wherein the step of anisotropically removing said insulator further comprises the step of directionally etching said insulator.

18. The method of claim 14, wherein the step of anisotropically removing is executed using reactive ion etching.

19. The method of claim 14, further comprising the steps of:

choosing for said insulator a positive-tone photosensitive material;

blanket exposing to light said positive-tone photosensitive material; and

developing said positive-tone photosensitive material,

whereby said positive-tone photosensitive material is readied for the step of removing

anisotropically.

20. The method of claim 14, wherein the step of anisotropically removing said insulator further comprises the step of additional thinning said insulator underneath said T-bar portion.

21. The method of claim 14, further comprising the step of employing low-k materials for said insulator.

22. The method of claim 21, further comprising the step of choosing said low-k materials from compounds of materials selected from the group consisting of SiCO, SiCOH, SiCH, these silicon containing materials with Si up to 100% replaced by Ge and these silicon containing materials further containing atoms of materials selected from the group consisting of N and F.

23. The method of claim 21, further comprising the step of choosing said low-k materials from materials selected from the group consisting of diamond-like carbon, fluorinated amorphous carbon, insulating inorganic oxides, inorganic polymers, organic polymers, photosensitive polymers, photosensitive polyimides and photosensitive amorphous fluorocarbons.

24. A method for producing a high performance MODFET comprising an enhanced T-gate, comprising the steps of:

fabricating a free T-gate, said free T-gate having a neck portion and a T-bar portion;

coating conformally said free T-gate with an insulator;

removing anisotropically said insulator by using said T-bar portion for masking, wherein leaving said insulator only underneath said T-bar portion; and

employing a self-aligned source/drain metallurgy, wherein said insulator forms a borderline for said metallurgy.

25. The method of claim 24, further comprising the step of:

additional thinning of said insulator underneath said T-bar portion.

26. The method of claim 24, wherein the step of employing said self-aligned source/drain metallurgy comprises the step of using angled deposition of a metal.

27. A method for manufacturing an integrated circuit comprising the steps of:

producing at least one high performance MODFET in said circuit, said step of producing further comprising the steps of:

fabricating a free T-gate, said free T-gate having a neck portion and a T-bar portion;

coating conformally said free T-gate with an insulator;

removing anisotropically said insulator by using said T-bar portion for masking, wherein leaving said insulator only underneath said T-bar portion; and

employing a self-aligned source/drain metallurgy, wherein said insulator forms a borderline for said metallurgy.

28. The method of claim 27, further comprising the step of:

depositing non-conformally an interconnect dielectric, whereby leaving gaps underneath said T-bar portion.

29. The method of claim 27, further comprising the step of employing a multilevel interconnect structure with low-k interconnect dielectrics.

30. The method of claim 29, further comprising the step of choosing said low-k interconnect dielectrics from materials selected from the group consisting of SiCO, SiCOH, SiCH, these silicon containing materials with Si up to 100% replaced by Ge, diamond-like carbon, fluorinated amorphous carbon, insulating inorganic oxides, inorganic polymers and organic polymers.